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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,815	11/21/2003	Frantisek Gasparik	LSI.86US01 (03-2045)	3313
24319	7590	08/11/2005	EXAMINER	
LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 MILPITAS, CA 95035			SIEK, VUTHE	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/719,815	Applicant(s) GASPARIK, FRANTISEK	
	Examiner Vuthe Siek	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. This office action is in response to application 10/719,815 filed on 11/21/2003.

Claims 1-4 remain pending in the application.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because the abstract is not descriptive. Correction is required. See MPEP § 608.01(b).

Appropriate correction is required.

Claim Objections

3. Claims 1-4 are objected to, in steps of "calculating the inductance of the individual traces; and calculating the capacitance of the individual traces", it is sure which ones the inductance and capacitance. Clarification is requested.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

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The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-4 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The steps of calculating the inductance and calculating crosstalk are not described in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Tallinger et al., "Tools for on-chip interconnect inductance extraction", August 2002, pp. 1-6.

8. As to claims 1-4, Tallinger teach substantially similar claimed invention comprising analyzing the effects of crosstalk in a circuit that includes a bond wire and a package (see entire document). The accurate package modeling includes bond wire and a package having RLC models. The method comprises modeling the bond wire with an equivalent bond wire resistance, equivalent bond wire capacitance and

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equivalent bond wire inductance; modeling the package with an equivalent bond wire resistance, equivalent package capacitance and equivalent package inductance; calculating the inductance of individual traces of the bond wire and package using an inductance matrix in which diagonal elements of the inductance matrix represent self-inductance of individual traces of the bond wire and package and non-diagonal elements of the inductance matrix represent mutual inductance between any two of the individual traces of the bond wire and package; calculating the capacitance of individual traces of the bond wire and package using a capacitance matrix in which diagonal elements of the capacitance matrix represent total capacitance of individual traces of the bond wire and package and non-diagonal elements of the capacitance matrix represent capacitance between any two of the individual traces of the bond wire and package; calculating crosstalk of the circuit created by the bond wire and package as a result of the inductance calculated by the inductance matrix and the capacitance calculated using the capacitance matrix (Tallinger et al. teach a complete solution to calculate self-and mutual inductances in a matrix representation; the matrix representation must comprise self-inductance of individual traces in diagonal elements and mutual inductance of individual traces in non-diagonal elements; similar form of matrix is implemented for capacitance matrix representation).

9. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by TDA, TDA Systems, Inc., "High0Density Interconnecct (HDI) Magazine, March 2001, pp. 1-16.

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10. As to claims 1-4, TDA teaches a method/system of analyzing the effects of crosstalk in a circuit that includes a bond wire and a package and in a high frequency integrated transmission system comprising modeling the bond wire and package with an equivalent bond wire/package resistances, capacitances and inductances; calculating the inductance in individual traces of the bond wire and package using an inductance matrix in which diagonal elements represents self-inductance of individual traces and non-diagonal elements represent mutual inductance between any two of the individual traces; calculating the capacitance of individual traces of the bond wire and package using a capacitance matrix in which diagonal elements represent total capacitance of individual traces and non-diagonal elements represent capacitance between any two of individual traces; calculating crosstalk of the circuit created by the bond wire and package as a result of the inductance calculated by the inductance matrix and the capacitance calculated using the capacitance matrix (See entire document).

11. Related prior art: applicant is requested to consider these below reference entirely. Sercu et al., "EXPERIMENTAL CIRCUIT MODEL GENERATION OF NON-UNIFORM COUPLED MULTI-CONDUCTOR STRUCTURES," IEEE, 1997, PP. 1781-1784; Beker, "Numral and Experimental Modeling of High-Speed Cables and Interconnets," IEEE, 1997, pp. 898-904; Larry Smith, "Simultaneous Switch Noise and Power Plane Bounce for CMOS Technology," IEEE, 1999, pp. 163-166.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek


VUTHE SIEK
PRIMARY EXAMINER